

SENSE AMPLIFIER SYSTEMS AND METHODS

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5

TECHNICAL FIELD

The present invention relates generally to electrical circuits and, more particularly, to sense amplifiers.

BACKGROUND

10 Sense amplifiers are employed in a variety of applications to monitor data signals and provide output signals based on the data signals. For example, a sense amplifier typically is utilized in a memory array to read data from one or more bitlines. The bitlines are generally routed from a memory cell
15 in the memory array to the sense amplifier via column decode pass gates. The Sense amplifier reads the data and provides its output, which completes the read process.

One drawback of some conventional sense amplifier applications, such as for example for a memory array, is the
20 relatively long time delay from the start of a read to the start of the next read (i.e., read cycle time). One technique to reduce the amount of time required to complete a read cycle is to precharge the bitlines prior to each read. However, typically there is still a relatively long read cycle time,
25 especially with large memory arrays having significant signal propagation delays. As a result, there is a need for improved sense amplifier techniques.

SUMMARY

Systems and methods are disclosed herein to provide sense amplifiers for various applications. For example, in accordance with an embodiment of the present invention, a sense amplifier
5 is disclosed having an associated precharge circuit and a read completion detection circuit. The precharge circuit and the read completion detection circuit reduce the amount of time required to complete a read cycle as compared to some conventional sense amplifier circuits. Additional logic
10 circuits may be provided to provide the desired application granularity so that the techniques disclosed herein may apply, for example, to one, four, eight, or more bits at a time.

More specifically, in accordance with one embodiment of the present invention, a sense amplifier circuit includes a sense
15 amplifier coupled to a first input line and a second input line and adapted to receive an enable signal, wherein the enable signal controls whether the sense amplifier is enabled; a first inverter coupled to the first input line and adapted to provide a first output signal; a second inverter coupled to the second
20 input line and adapted to provide a second output signal; and a logic gate adapted to receive the first output signal and the second output signal and to provide a trip signal.

In accordance with another embodiment of the present invention, a memory array includes a plurality of sense
25 amplifiers adapted to read data provided on bitlines; a plurality of corresponding precharge circuits adapted to precharge the bitlines coupled to the sense amplifiers; a plurality of corresponding inverters coupled to the bitlines and adapted to provide output signals based on signal levels on the
30 bitlines coupled to the sense amplifiers; a plurality of corresponding logic gates adapted to receive the output signals from the corresponding inverters and to provide trip signals

based on the output signals; and a plurality of corresponding latches adapted to store the output signals from one of the corresponding inverters under control of the corresponding trip signals, wherein the trip signals transition to a first value
5 when the corresponding bitlines are precharged and transition to a second value when the corresponding sense amplifiers read the data on the corresponding bitlines.

In accordance with another embodiment of the present invention, a method of reading data from data lines includes
10 disabling a sense amplifier coupled to the data lines; precharging the data lines; providing a first signal value via inverters coupled to the data lines when the data lines are precharged; providing the data on the data lines after the first signal value is provided; enabling the sense amplifier to read
15 the data placed on the data lines after the first signal value is provided; and providing a second signal value via the inverters coupled to the data lines when the sense amplifier has read the data placed on the data lines.

The scope of the invention is defined by the claims, which
20 are incorporated into this section by reference. A more complete understanding of embodiments of the present invention will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration of the following detailed description of one or more
25 embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a circuit diagram utilizing a sense amplifier
30 in accordance with an embodiment of the present invention.

Fig. 2 shows an exemplary circuit for a portion of the circuit diagram of Fig. 1 in accordance with an embodiment of the present invention.

Fig. 3 shows an exemplary circuit for a portion of the circuit diagram of Fig. 1 in accordance with an embodiment of the present invention.

Fig. 4 shows a block diagram of a sense amplifier application in accordance with an embodiment of the present invention.

Fig. 5 shows a circuit diagram for a portion of the block diagram of Fig. 4 in accordance with an embodiment of the present invention.

Fig. 6 shows a state diagram for the circuit diagram of Fig. 5 in accordance with an embodiment of the present invention.

Embodiments of the present invention and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

DETAILED DESCRIPTION

Fig. 1 shows a circuit 100 in accordance with an embodiment of the present invention. Circuit 100 represents, for example, a portion of a memory array and illustrates certain aspects of the present invention. However, it should be understood that one or more of the techniques disclosed herein are applicable to a number of different types of sense amplifier applications,

such as for example for sense amplifier applications within a product term circuit of a programmable logic device.

Circuit 100 includes logic gates 102, 104, 106, and 108, precharge circuits 110 and 112, a sense amplifier 114, a latch
5 116, pass gates 122, and inverters 124 and 126. In terms of general operation, when a column select signal 128 and an enable signal 130 are asserted (e.g., a logical high level), logic gate 102 (e.g., a NAND gate) switches on pass gates 122, while logic gate 104 (e.g., a NAND gate) switches off precharge circuit 112
10 and switches on sense amplifier 114 via an enable signal 138 to initiate a read operation of bitlines 118 and 120 by sense amplifier 114.

Precharge circuit 110, in general, is switched off at approximately the same time as when precharge circuit 112 is
15 switched off to allow sense amplifier 114 to read the values on bitlines 118 and 120 from the selected memory cell (not shown). Precharge circuit 110 is switched on to precharge bitlines 118 and 120 (e.g., globally within the memory array of which circuit 100 forms a part of) after the completion of a read cycle (e.g.,
20 after all trip signals, such as a trip signal 134 described herein, are asserted and the selected word line for the read cycle has been deasserted). In general, bitlines 118 and 120 (e.g., globally and locally to sense amplifier 114) must be precharged prior to each read by sense amplifier 114.

25 Inverters 124 and 126 are coupled to bitlines 118 and 120 leading into sense amplifier 114 and, along with logic gate 106 (e.g., a NOR gate), form a read completion detection circuit. A trip signal 136 provided by logic gate 106 transitions to a logical low level (or its complement, a trip signal 134,
30 transitions to a logical high level) once a read operation is completed by sense amplifier 114. Trip signal 136 remains at a logical low level until the precharging is completed by

precharge circuit 112 of bitlines 118 and 120 (i.e., at the input to sense amplifier 114).

Inverters 124 and 126 help to isolate sense amplifier 114 from large capacitive loads and to provide their outputs (labeled DOUTB and DOUT, respectively) to logic gate 106. Inverters 124 and 126 are placed between bitlines 118 and 120 and logic gate 106 to reduce parasitic capacitances. For example, a logic gate (e.g., a NAND gate) connected directly to bitlines 118 and 120 (i.e., inverters 124 and 126 not implemented) would typically have parasitic capacitances associated with its n-channel field effect transistors (NFETS) that couple to nodes with different potentials within the logic gate and, consequently would not present identical loads to bitlines 118 and 120. Thus, there is the possibility of biasing sense amplifier 114, which could result in erroneous reads due to sense amplifier 114 tripping in one direction more easily than the other.

The output signal (labeled DOUT) from inverter 126 is also provided to latch 116 (e.g., a D flip flop), while trip signal 134 is utilized as a clock for latch 116. Latch 116 may also receive a reset signal 132 (e.g., a global reset). Latch 116 stores the result of a read operation by sense amplifier 114 and provides the result as an output signal 140.

By storing the result in latch 116, the precharge cycle for the next read operation can begin immediately. For example, when trip signal 136 transitions to a logical low level, enable signal 130 may transition to a logical low level (e.g., deasserted), which results in logic gate 102 switching off pass gates 122 and logic gate 104 switching off sense amplifier 114 and switching on precharge circuit 112 to begin charging bitlines 118 and 120 locally at sense amplifier 114. Precharge circuit 110 would begin precharging bitlines 118 and 120

globally within the memory array, for example, once all of the sense amplifiers within the memory array have completed their read operation and the selected word line has been deasserted.

Fig. 2 shows a circuit 200, which is an exemplary circuit
5 implementation for sense amplifier 114 of Fig. 1 in accordance with an embodiment of the present invention. Circuit 200 includes two cross-coupled inverters whose connection to a reference voltage (e.g., ground) is opened when enable signal 138 is deasserted. Thus, when enable signal 138 is asserted,
10 circuit 200 performs a read operation of bitlines 118 and 120.

Fig. 3 shows a circuit 300, which is an exemplary circuit implementation for precharge circuit 112 of Fig. 1 in accordance with an embodiment of the present invention. Circuit 300 may also be an exemplary circuit implementation for precharge
15 circuit 110, but its control signal would generally differ (i.e., enable signal 138 would be replaced, such as by a control signal 142 labeled BL_PCHG_B in Fig. 1) and transistor sizes may differ (e.g., transistor sizes for precharge circuit 110 would increase relative to precharge circuit 112), depending upon the
20 size of the memory array with precharge circuit 110 generally having to precharge a longer portion of bitlines 118 and 120 than precharge circuit 112.

In general terms, circuit 100 includes a read completion detection circuit and a self-timed precharge circuit. Thus,
25 circuit 100 detects when sense amplifier 114 has read a bit (also referred to as when sense amplifier 114 has tripped) on bitlines 118 and 120 (i.e., trip signal 136 transitions to a logical low level). Circuit 100 also detects when the inputs to sense amplifier 114 have completed their precharge cycle (i.e.,
30 when precharge circuit 112 has locally precharged bitlines 118 and 120 at sense amplifier 114) by monitoring trip signal 136

for a transition to a logical high level (or by monitoring its complement, trip signal 134).

It should be understood that circuit 100 may be extended to select from a number of bitline pairs. For example, column
5 select signal 128 may represent complementary signals (as indicated by <1:0> notation in Fig. 1 and by a similar notation for other elements in Fig. 1), with logic gate 102 representing two logic gates, pass gates 122 representing two pairs of pass gates, and bitlines 118 and 120 representing two pairs of
10 bitlines. Thus, the two pairs of pass gates 122 form a column multiplexer, which is controlled to select which pair of bitlines to route to sense amplifier 114. Precharge circuit 110 may also represent two precharge circuits, one for each pair of bitlines. Enable signal 130 would be fed to both logic gates
15 represented by logic gate 102, with one of the column select signals routed to one logic gate and the complement routed to the other logic gate. In general, the description herein may reference certain figure elements (e.g., logic gate 102, pass gates 122, etc.) in a singular sense, but it should be
20 understood that a number of these figure elements may be implemented, for example, to accommodate the selection of any number of bitline pairs to route to sense amplifier 114 in accordance with one or more embodiments of the present invention.

25 More than one sense amplifier 114 may be controlled by a control circuit (e.g., a sense amplifier controller). For example, depending on the actual granularity (e.g., a bit, a nibble, or a word) of the sense amplifier controllers for sense amplifiers 114 within the memory array, this technique may
30 reduce the read precharge cycle time by eliminating the signal propagation delays associated with large memory arrays.

As an example, Fig. 4 shows a block diagram 400 for sense amplifier control in accordance with an embodiment of the present invention. In this exemplary implementation, a block 402 represents a sense amplifier controller, which provides an enable signal 414 to four sense amplifiers circuits (e.g., enable signal 414 corresponding to enable signal 130 is provided to control four of circuits 100) represented by a block 404 (i.e., block 404 represents four sense amplifier circuits, as indicated by the notation <3:0>, with each sense amplifier circuit selecting between two pairs of bitlines). For this example, block 402 controls the reading of four bits (i.e., a granularity of a nibble).

Block 402 receives a read enable signal 406, a reset signal 408, four trip signals 410, and four trip signals 412 (corresponding complements of trip signals 410) and provides enable signal 414 to block 404. Read enable signal 406 may be delayed appropriately so that sense amplifiers within block 404 are not enabled before their associated bitlines have started to separate in terms of their voltage. Reset signal 408 may be a global reset signal (e.g., the same signal as reset signal 132 of Fig. 1). Trip signals 410 and 412 provide true and complement trip signals from completion detection circuits within block 404, whose operation is as described similarly in reference to Fig. 1 for trip signals 134 and 136.

Block 404 provides trip signals 410 and 412, as discussed above, along with four output signals 416 and receives four control signals 418, two column select signals 420, reset signal 408, and eight bitlines 422 and 424. Output signals 416 provide the results from the four sense amplifiers as described similarly in reference to Fig. 1 for output signal 140. Similarly, control signals 418, column select signals 420, and bitlines 422 and 424 operate in a similar fashion as described

similarly in reference to Fig. 1 for control signal 142, column select signal 128, and bitlines 118 and 120, respectively.

Fig. 5 shows a circuit 500, which is an exemplary circuit implementation for block 402 of Fig. 4 in accordance with an embodiment of the present invention. Fig. 6 shows a state diagram 600 for circuit 500 of Fig. 5 in accordance with an embodiment of the present invention. In general, the appropriate signal may be chosen from trip1, trip2, trip3, and trip4 signals shown in Fig. 5 for state diagram 600, based on whether all of the trip signals should be logically high or logically low for a desired state transition and on the polarity required. Also, the signals listed to the left of the slash "/" indicate a transition or input, while the signals listed to the right of the slash "/" indicate a result of the transition or the input as a transition from one state to the next occurs.

For example, a transition from state zero to state three occurs if reset signal 408 is asserted, with a return to state zero when reset signal 408 is deasserted. As another example, when read enable signal 406 is asserted, enable signal 414 is asserted and a transition to state one occurs.

In general, when a transition to state one occurs, the column pass gates are enabled, the precharge circuits are switched off, and the sense amplifiers are switched on. When a transition to state two occurs (i.e., the trip signals from the monitored sense amplifiers are asserted), the sense amplifiers are switched off and the precharge of the bitlines begins again. When the precharge of the bitlines is completed, the trip signals are deasserted and a transition to state six occurs followed by a transition to state zero when read enable signal 406 is deasserted.

For the exemplary implementation described in reference to Figs. 4 through 6, as an example, the trip signals from four adjacent bits (i.e., a nibble) may be fed to a single sense amplifier enable state machine. This level of granularity may
5 accommodate various memory configurations of the memory array. Other levels of granularity, however, may be implemented based on one or more embodiments of the present invention and on the requirements of the desired application. In general, one of the basic functions of the sense amplifier enable state machine is
10 to appropriately assert the enable signal when a read enable input signal is asserted, and appropriately deassert the enable signal when all of the trip signals are asserted (as described herein).

An exemplary basic sequence of events may be described, in
15 accordance with an embodiment of the present invention, for a memory array implementing certain aspects of the present invention as described herein. First, a new read address and the read enable signal are latched into their input registers by a read clock. While the read address is decoded and the correct
20 wordline is enabled, the registered read enable signal is delayed by a similar amount of time so that the sense amplifier is not enabled before the bitlines have started to separate in terms of their voltage.

The delayed read enable signal (e.g., read enable signal
25 406) is then received by a sense amplifier enable state machine (e.g., block 402), which enables a column multiplexer to connect the correct column bitlines to the local sense amplifier bitlines and terminates the precharge of the sense amplifier bitlines. The sense amplifier (e.g., sense amplifier 114)
30 evaluates the bitlines and provides non-inverted and inverted data signals to the pair of inverters (e.g., inverters 124 and 126) that feed the NOR gate (e.g., logic gate 106). Because

both bitlines were precharged high, the inverter outputs are both low at the start of the read.

As the data on the bitlines is resolved by the sense amplifier, either the DOUT or the DOUTB signal (from the
5 respective inverters) goes high. This results in the output of the NOR gate to drop, which drives the trip signal (e.g., trip signal 134) high and latches the data into the output latch (e.g., latch 116). When all four of the trip signals going to the sense amplifier enable state machine have gone high, the
10 column multiplexers are disabled, causing the precharge cycle to begin.

When the trip signal farthest from the read enable register transitions high, the read enable register is cleared, resulting in the registered read enable signal to go low. Once the sense
15 amplifier precharge cycle is complete, the trip signal will go low, signaling the sense amplifier enable state machine that the sense amplifier is ready for the next read cycle.

Embodiments described above illustrate but do not limit the invention. It should also be understood that numerous
20 modifications and variations are possible in accordance with the principles of the present invention. Accordingly, the scope of the invention is defined only by the following claims.